PACT FPGA Patents

	Patent	Headline	Link	Notes
US	8 195 856	I/O and memory bus system for DFPS and units with two- or multi-dimensional programmable cell architectures	http://www.google.com/patents/US8195856	
US	8 156 312	Processor chip for reconfigurable data processing, for processing numeric and logical operations and including function and interconnection control units	http://www.google.com/patents/US8156312	
US	8 099 618	Methods and devices for treating and processing data	http://www.google.com/patents/US8099618	
US	8 058 899	Logic cell array and bus system	http://www.google.com/patents/US8058899	
US	7 899 962	I/O and memory bus system for DFPs and units with two- or multi-dimensional programmable cell architectures	http://www.google.com/patents/US7899962	
US	7 844 796	Data processing device and method	http://www.google.com/patents/US7844796	
US	7 822 968	Circuit having a multidimensional structure of configurable cells that include multi-bit-wide inputs and outputs	http://www.google.com/patents/US7822968	
US	7 822 881	Process for automatic dynamic reloading of data flow processors (DFPs) and units with two- or three- programmable cell architectures (FPGAs, DFGAs, and the like)	http://www.google.com/patents/US7822881	
US	7 782 087	Reconfigurable sequencer structure	http://www.google.com/patents/US7782087	
US	7 650 448	I/O and memory bus system for DFPS and units with two- or multi-dimensional programmable cell architectures	http://www.google.com/patents/US7650448	
US	7 595 659	Logic cell array and bus system	http://www.google.com/patents/US7595659	
US	7 565 525	Runtime configurable arithmetic and logic cell	http://www.google.com/patents/US7565525	
US	7 444 531	Methods and devices for treating and processing data	http://www.google.com/patents/US7444531	
US	7 337 249	I/O and memory bus system for DFPS and units with two- or multi-dimensional programmable cell architectures	http://www.google.com/patents/US7337249	
US	7 237 087	Reconfigurable multidimensional array processor allowing runtime reconfiguration of selected individual array cells	http://www.google.com/patents/US7237087	
US	7 174 443	Run-time reconfiguration method for programmable units	http://www.google.com/patents/US7174443	
US	7 036 036	Method of self-synchronization of configurable elements of a programmable module	http://www.google.com/patents/US7036036	reissue
US	7 028 107	Process for automatic dynamic reloading of data flow processors (DFPS) and units with two- or three-dimensional programmable cell architectures (FPGAs, DFGAs, and the like)	http://www.google.com/patents/US7028107	
US	6 968 452	Method of self-synchronization of configurable elements of a programmable unit	http://www.google.com/patents/US6968452	
US	6 859 869	Data processing system	http://www.google.com/patents/US6859869	
US	6 728 871	Runtime configurable arithmetic and logic cell	http://www.google.com/patents/US6728871	
US	6 721 830	I/O and memory bus system for DFPS and units with two- or multi-dimensional programmable cell architectures	http://www.google.com/patents/US6721830	
US	6 542 998	Method of self-synchronization of configurable elements of a programmable module	http://www.google.com/patents/US6542998	
US	6 526 520	Method of self-synchronization of configurable elements of a programmable unit	http://www.google.com/patents/US6526520	
US	6 513 077	I/O and memory bus system for DFPS and units with two- or multi-dimensional programmable cell architectures	http://www.google.com/patents/US6513077	
US	6 477 643	Process for automatic dynamic reloading of data flow processors (DFPS) and units with two- or three-dimensional programmable cell architectures (FPGAs, DFGAs, and the like)	http://www.google.com/patents/US6477643	
US	6 425 068	Unit for processing numeric and logic operations for use in central processing units (CPUs), multi processor systems, data-flow processors (DSPs), systolic processors and field programmable gate arrays (EPGAs)	http://www.google.com/patents/US6425068	what is EPGA ?

US	6 338 106	I/O and memory bus system for DFPS and units with two- or multi-dimensional programmable cell architectures	http://www.google.com/patents/US6338106	
US	6 119 181	I/O and memory bus system for DFPS and units with two- or multi-dimensional programmable cell architectures	http://www.google.com/patents/US6119181	
US	6 088 795	Process for automatic dynamic reloading of data flow processors (DFPS) and units with two- or three-dimensional programmable cell architectures (FPGAs, DFGAs, and the like)	http://www.google.com/patents/US6088795	
US	6 081 903	Method of the self-synchronization of configurable elements of programmable unit	http://www.google.com/patents/US6081903	
US	6 021 490	Run-time reconfiguration method for programmable units	http://www.google.com/patents/US6021490	
US	5 943 242	Dynamically reconfigurable data processing system	http://www.google.com/patents/US5943242	

PACT FPGA Applications

	Application	Notes
	11/820,780	allowed (patent US 8 156 312)
	12/884,042	
	12/840,742	allowed (patent US 8 195 856)
	12/367,055	
	12/389,155	
	12/109,280	
	12/909,061	
	12/909,150	
	12/909,203	
	12/720,898	
	12/840,559	
	12/389,116	
	13/289,296	
	13/023,796	
	12/247,076	
	12/389,274	